Analyzing the Contact-Doping Effect in In_2O_3 FETs: Unveiling the Mechanisms Behind the Threshold-Voltage Roll-Off in Oxide Semiconductor Transistors

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***Abstract*—In this work, the contact-doping effect (CDE) and its impact on the threshold voltage (V_T) roll-off in indium oxide (In_2O_3) field-effect transistors (FETs) are systematically studied. By analyzing the long channel length (L_{ch}) and short L_{ch} devices separately using a modified transfer length method (TLM), ΔL can be extracted to quantify the CDE. The correlation between ΔL and the L_{ch} at which V_T roll-off occurs suggests that CDE may be a key factor contributing to the V_T roll-off in In_2O_3 transistors. Next, the underlying mechanisms of CDE are investigated. It is found that oxygen scavenging reactions (OSRs) during the deposition of source/drain (S/D) metals on the In_2O_3 channel is one of the reasons behind CDE. S/D metals can scavenge oxygen atoms from In_2O_3, creating oxygen vacancies and increasing the carrier density near the S/D regions. Additionally, the Schottky barrier height (Φ_{SB}) of metal/In_2O_3 contacts might also influence the CDE: a positive Φ_{SB} depletes carriers, while a negative Φ_{SB} accumulates them in the In_2O_3 channel under the S/D. This study provides a new approach to investigating CDE and highlights its critical role in understanding the V_T roll-off in oxide semiconductor (OS) transistors.**

***Index Terms*—contact-doping effect (CDE), indium oxide (In_2O_3), oxygen scavenging reaction (OSR), Schottky barrier height, threshold voltage roll-off.**

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I. Introduction

INDIUM oxide (In_2O_3) based oxide semiconductor (OS) field-effect transistors (FETs) have gained increasing research attention in recent years due to their promising application for monolithic 3-D integration (M3DI) [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15]. The concept of M3DI is to directly grow and fabricate semiconductor devices on top of an already processed front-end-of-line (FEOL) layer, such as silicon logic devices or chips [1], [16]. This approach enhances chip performance in two ways: *more Moore* and *more than Moore*. First, M3DI increases the device density per area by stacking additional transistors above the FEOL layer (*More Moore*) [7], [14]. Second, it enables heterogeneous integration of various semiconductor devices—such as radio frequency (RF) [17], [18], memory [15], and power devices [19]—to enhance chip functionality (*More than Moore*).

A key challenge in achieving M3DI is the strict back-end-of-line (BEOL) thermal budget, which typically requires processing temperatures below 400 °C [1]. Fortunately, OSs can be deposited and further processed at temperatures below this limit, making them excellent candidates for M3DI [5]. Among various OS FETs, atomic-layer-deposited (ALD) In_2O_3 FETs offer several advantages, including excellent conformality and uniformity on 3-D structures [5], high electron mobility of 152 $cm^2/(V\cdot s)$ [20], ultrahigh ON-current (~20 mA/μm) in gate-all-around structure [21], good reliability [13], and ultralow contact resistance (R_C) of 23.4 $\Omega\cdot\mu$m, approaching the quantum limit of metal/semiconductor contacts [8], [22].

The channel length (L_{ch}) dependent threshold voltage (V_T)—specifically, the V_T roll-off phenomenon as the L_{ch}

decreases—has been widely reported in In_2O_3 and doped-In_2O_3 [e.g., InSnO, InZnO (IZO), InGaO (IGO), and InGaZnO (IGZO)] FETs [4], [6], [9], [12], [18], [22], [23], [24], [25], [26], [27]. While many studies have investigated methods to mitigate V_T roll-off, relatively few have explored the underlying mechanisms responsible for the L_{ch}-dependent V_T shifts in In_2O_3-based FETs [23]. A common assumption is that this roll-off stems from the short-channel effect (SCE), which occurs when electrostatic control of gate to channel weakens as the source/drain (S/D) spacing or L_{ch} shrinks. However, most In_2O_3-based FETs are thin-film transistors (TFTs) with channel thickness far below 10 nm [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [18], [26]. In such ultrathin channels, strong gate control should effectively suppress the traditional SCE in the investigated L_{ch} range (≥40 nm). This suggests that the observed V_T roll-off in In_2O_3-based TFTs is driven by mechanisms beyond conventional SCE.

In this work, we propose that the contact-doping effect (CDE) is responsible for the V_T roll-off in In_2O_3 FETs. Using a modified transfer length method (TLM), we systematically investigate and verify the relationship between CDE and V_T roll-off. Additionally, by varying S/D metal materials, we explore the physical mechanisms underlying CDE. This research offers new insights into CDE and its influence on V_T roll-off, emphasizing its significance in the design and optimization of aggressively scaled OS transistors.

II. Experiments and Simulations

Fig. 1(a) illustrates the schematic of the back-gate (BG) In_2O_3 transistors analyzed in this study, and Fig. 1(b) outlines the fabrication process. The process began with the deposition of 6 nm Al_2O_3 adhesion layer via ALD at 175 °C on SiO_2/Si substrate, followed by 60 nm Ni BG deposited through electron-beam evaporation. Next, 4 nm HfO_2 gate dielectric was deposited by ALD at 200 °C. In_2O_3 with channel thickness (T_{ch}) ranging from 1.2 to 2.0 nm was used as transistor channel and was grown by ALD at 225 °C. Various metals were then deposited by electron-beam evaporation to serve as the S/D electrodes, as listed in Fig. 1(c). Different S/D materials were employed to investigate the CDE in In_2O_3 transistors. Finally, channel isolation and the definition of transistor channel width (W_{ch}) of 1 μm were achieved through inductively coupled plasma (ICP) etching using Ar/BCl_3 plasma. For the ALD processes above, $Al(CH_3)_3$ (TMA), $[(CH_3)_2N]_4Hf$ (TDMAHf), $(CH_3)_3In$ (TMIn), and H_2O were used as Al, Hf, In, and O precursors, respectively. Fig. 1(d) shows a cross-sectional scanning transmission electron microscopy (STEM) image with energy-dispersive X-ray spectroscopy (EDS) elemental mapping of an In_2O_3 FET with Ni as the S/D material, while Fig. 1(e) presents the corresponding image for a device with Pt as S/D.

Electrical characterizations were conducted at room temperature in a Cascade probe station under an N_2 ambient using the Keysight B1500A system. The V_T of the devices was determined via the linear extrapolation method based on their transfer characteristics.

To investigate the oxygen interstitial formation energy for different metals, *ab initio* calculations were performed using the QuantumATK software with the GGA-PBE functional and

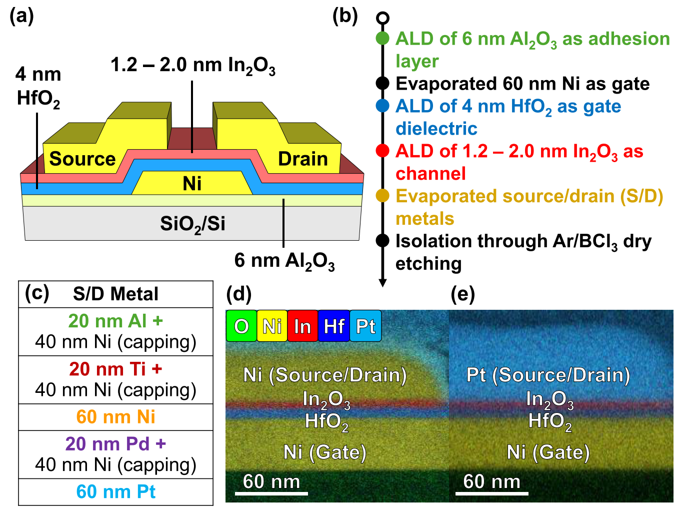

Fig. 1. (a) Schematic device structure of BG In_2O_3 transistors. (b) Fabrication process flow of BG In_2O_3 FETs. (c) List of S/D metals used in this work. Different S/D metals were utilized to study the CDE in In_2O_3 devices. Cross-sectional STEM image with EDS elemental mappings of In_2O_3 FETs with (d) Ni as S/D and (e) Pt as S/D.

PseudoDojo basis sets. Oxygen atoms were placed at interstitial sites, identified based on the lowest energy configuration.

III. Results and Discussion

A. Quantification of the CDE

Fig. 2 presents the transfer characteristics of In_2O_3 FETs with different L_{ch}, Ni as the S/D metal, and T_{ch} = 1.2, 1.6, and 2.0 nm. Noticeable V_T roll-off is observed as the L_{ch} decreases from 1000 to 40 nm across all T_{ch} conditions. To elaborate, for T_{ch} = 1.2 and 1.6 nm, the I_D–V_{GS} curves exhibit a negative shift when L_{ch} falls below 600 nm [Fig. 2(a) and (b)]. For T_{ch} = 2.0 nm, a similar leftward shift is observed when L_{ch} is reduced to below 200 nm [Fig. 2(c)]. The V_T roll-off observed in Fig. 2 is unlikely to be caused by the traditional SCE. SCE can be quantified by the natural length theory of MOSFETs [28], [29]. The natural length (λ) of silicon-on-insulator (SOI) MOSFETs—whose structure is similar to BG In_2O_3 FETs—is given by

$$\lambda = \sqrt{\frac{\varepsilon_{ch}}{\varepsilon_{ox}} \cdot T_{ch} \cdot T_{ox}} \quad (1)$$

where ε_{ch} is the dielectric constant of the channel material (In_2O_3 with ε_{ch} = 8.9 [3]), ε_{ox} is the dielectric constant of the gate oxide (HfO_2 with $\varepsilon_{ox} \sim 8.6$, calculated based on the measured gate oxide capacitance of 1.9×10^{-6} F/cm^2), T_{ch} is the channel thickness, and T_{ox} is the gate oxide thickness (T_{ox} = 4.0 nm). For our In_2O_3 devices with T_{ch} = 1.2–2.0 nm, λ values are calculated to be 2–3 nm using (1), as shown in Fig. 3(a). Given that SCE should only become significant when $L_{ch} \leq 5 \times \lambda$ = 10–15 nm [29], the In_2O_3 transistors in this study should remain unaffected by the SCE since the gate control over the channel center is still stronger than the control from S/D. However, the calculated 5 × λ values contradict our experimental observations of V_T roll-off happening at L_{ch} below 600 nm (Fig. 2). This discrepancy suggests that the roll-off is not caused by SCE but rather by other reasons, such as CDE.

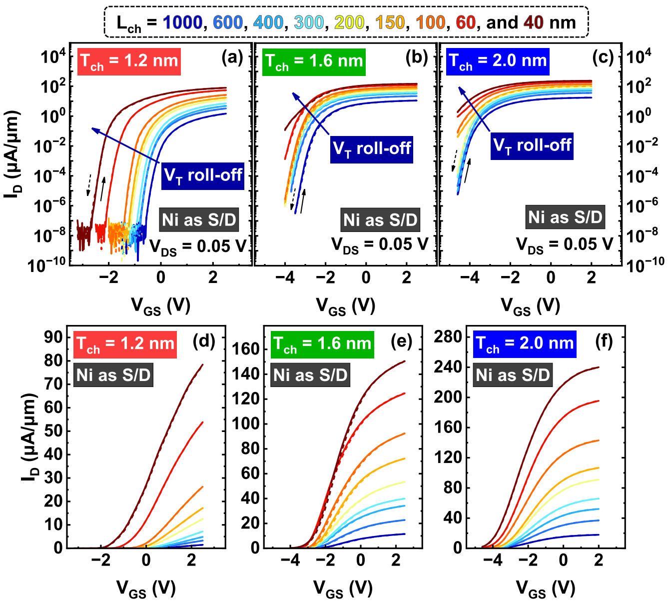

Fig. 2. Transfer characteristics of In_2O_3 transistors with Ni as S/D metal, channel length (L_{ch}) = 1 μm – 40 nm, and channel thickness (T_{ch}) of 1.2 nm [(a): I_D in log scale; (d): I_D in linear scale], 1.6 nm [(b): I_D in log scale; (e): I_D in linear scale], and 2.0 nm [(c): I_D in log scale; (f): I_D in linear scale]. Solid lines indicate V_{GS} sweeping forward, while dashed lines represent V_{GS} sweeping backward.

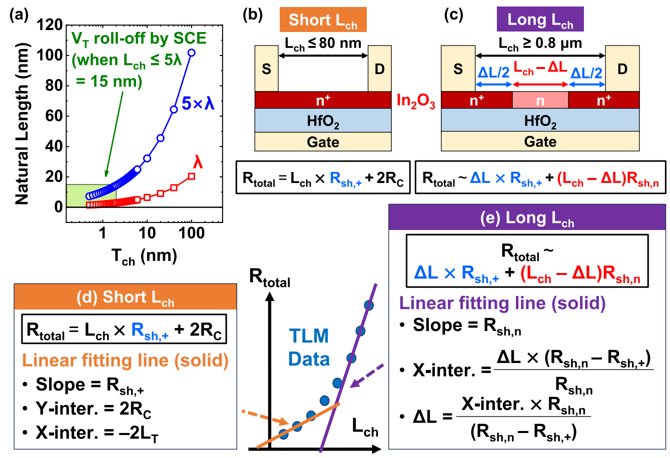

Fig. 3. (a) Calculated natural length (λ) as a function of T_{ch}. When L_{ch} is smaller than $5 \times \lambda$, V_T roll-off due to SCE is expected. For T_{ch} below 10 nm, the calculated λ remains under 6.5 nm, with $5 \times \lambda \leq 33$ nm. (b) and (c) Illustrate schematic cross sections of In_2O_3 transistors, showing carrier density profiles along the L_{ch} direction for short L_{ch} ($\leq$80 nm) and long L_{ch} ($\geq$0.8 μm) devices, respectively. The n^+ region represents a high carrier density area, while the n region corresponds to a medium carrier density area. ΔL denotes the length of the n^+ regions extending into the channel. R_{total} is the total channel resistance, with $R_{sh,+}$ and $R_{sh,n}$ representing the sheet resistances of the n^+ and n regions, respectively. If the carrier density in the In_2O_3 channel is nonuniform, the TLM analysis of R_{total}–L_{ch} data can be divided into two parts: (d) short L_{ch} segment, corresponding to the case of (b); (e) long L_{ch} segment, corresponding to the case of (c). Y-inter. and X-inter. represent the Y- and X-intercepts of the linear fitting lines, respectively. R_C is the contact resistance, and L_T is the transfer length.

It is suspected that the carrier density (i.e., electron density) within the In_2O_3 channel is non-uniform, with a higher carrier concentration near the S/D contacts compared to the channel center [Fig. 3(c)]. This phenomenon is referred to as CDE, as if the S/D contacts effectively increase the carrier density of the In_2O_3 channel under them. The non-uniform carrier distribution caused by CDE is illustrated in Fig. 3(b) and (c). Fig. 3(c) shows a schematic carrier density profile for In_2O_3 transistors with long L_{ch} ($\geq$0.8 μm), featuring n^+ (high electron density) regions near the S/D and an n (medium electron density) region at the channel center. ΔL is defined as the length of the n^+ regions extending into the channel, with $\Delta L/2$ contributed by the source and $\Delta L/2$ by the drain. When L_{ch} is sufficiently short ($\leq$80 nm), the n^+ regions from the S/D merge, as shown in Fig. 3(b). To extract the ΔL and quantify the CDE, a modified TLM is developed based on Fig. 3(b) and (c). From the long L_{ch} ($\geq$0.8 μm) devices, the total resistance (R_{total}) of the transistors can be written as

$$R_{total} \sim \Delta L \times R_{sh,+} + (L_{ch} - \Delta L) R_{sh,n} \tag{2}$$

where $R_{sh,+}$ is the sheet resistance of the n^+ region and $R_{sh,n}$ is the sheet resistance of the n region. Using (2), $R_{sh,n}$ can be extracted from the slope of the linear fitting lines in the long L_{ch} regime TLM analysis [Fig. 3(e)]. As for the short L_{ch} ($\leq$80 nm) devices, the R_{total} is given by

$$R_{total} = L_{ch} \times R_{sh,+} + 2R_C. \tag{3}$$

Utilizing (3), $R_{sh,+}$ can be determined from the slopes and R_C can be calculated from the Y-intercept of the linear fitting lines in the short L_{ch} regime [Fig. 3(d)]. By combining the $R_{sh,n}$ and $R_{sh,+}$, ΔL can be calculated using the following equation derived from (2):

$$\Delta L = \frac{X\text{-inter.} \times R_{sh,n}}{(R_{sh,n} - R_{sh,+})} \tag{4}$$

where X-inter. represents the X-intercept of the linear fitting lines in the long L_{ch} regime TLM analysis [Fig. 3(e)]. It should be noted that in the analysis of Fig. 3(b)–(e), the transition between n^+ and n regions is approximated as a step change to simplify the calculations and TLM analysis. A gradual transition from n^+ to n regions could be present, which may need to be considered for a more precise estimation of the CDE.

Fig. 4 presents the TLM analysis of total resistance (R_{total}) as a function of L_{ch} for In_2O_3 transistors with various T_{ch}. To accurately quantify the CDE, each set of R_{total}–L_{ch} data is analyzed at the same V_{GS} rather than the same V_{GS}–V_T. While adjusting R_{total}–L_{ch} data based on V_{GS}–V_T for each L_{ch} is a common practice to improve TLM linear fitting, particularly when V_T depends on L_{ch} [8], [25], [30], such normalization would exclude the information about CDE, as CDE itself is the potential cause of the V_T roll-off in In_2O_3 devices. For each T_{ch}, the R_{total}–L_{ch} data at a given V_{GS} is divided into two segments: short L_{ch} (40–80 nm) [Fig. 4(a), (c), and (e)] and long L_{ch} (0.8–1.0 μm) [Fig. 4(b), (d), and (f)], which are then analyzed using linear regression. According to the proposed TLM framework [Fig. 3(d) and (e)], $R_{sh,+}$ and $R_{sh,n}$ are extracted from the short- and long-L_{ch} regimes, respectively, as shown in Fig. 5(a)–(c). The extracted $R_{sh,+}$ values are

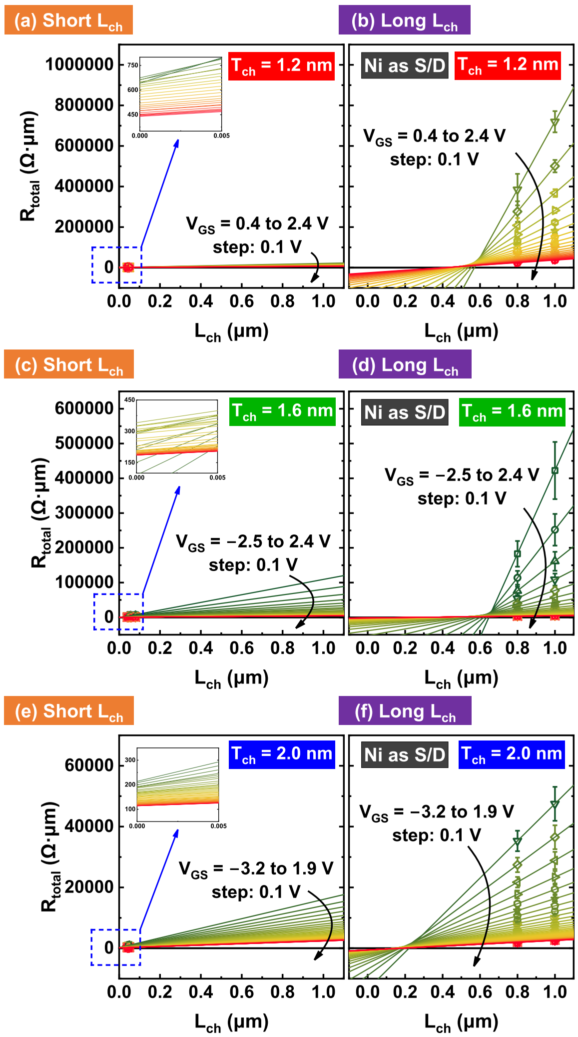

Fig. 4. TLM analysis of total resistance (R_{total}) versus L_{ch} for In_2O_3 FETs with different T_{ch} values: (a) and (b) 1.2 nm, (c) and (d) 1.6 nm, and (e) and (f) 2.0 nm. For each T_{ch}, the R_{total}–L_{ch} data is divided into two regions: short L_{ch} (40–80 nm) in (a), (c), and (e); long L_{ch} (0.8–1 μm) in (b), (d), and (f). Symbols represent experimental data, averaged over at least five devices. Solid lines indicate the linear fitting of the data. For the short L_{ch} regime [(a), (c), and (e)], $R_{sh,+}$ and R_C are extracted using the equations in Fig. 3(d) For the long L_{ch} regime [(b), (d), and (f)], $R_{sh,n}$ is extracted using the equation in Fig. 3(e).

consistently lower than $R_{sh,n}$ across all T_{ch}, confirming the presence of a non-uniform carrier density in the In_2O_3 channel.

Fig. 5(d) shows the extracted R_C as a function of V_{GS}, revealing that the R_C decreases as the T_{ch} increases. This behavior is linked to the transition from a positive to a negative Schottky barrier height (Φ_{SB}) at the metal/In_2O_3 contact [25], [31], as illustrated in Fig. 5(e). The quantum confinement effect (QCE) modifies the band structure of In_2O_3 as the T_{ch} becomes thinner [3], [25]. For instance, when T_{ch} is reduced from 1.6 to 1.2 nm, the QCE shifts the conduction band minimum (E_C) upward, moving it above the charge neutrality level (CNL) of In_2O_3. Due to strong Fermi-level pinning at the metal/In_2O_3 interface, the metal Fermi level (E_{FM}) remains close to the CNL of In_2O_3 [25]. Consequently, the alignment between E_C and CNL (which closely matches E_{FM}) dictates the value of Φ_{SB}. If E_C is above CNL (as in the case of T_{ch} =

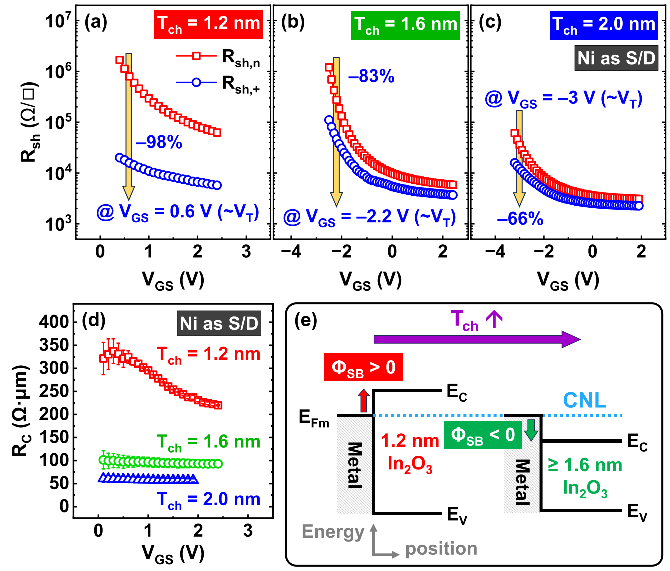

Fig. 5. Extracted $R_{sh,n}$ and $R_{sh,+}$ as a function of V_{GS} for In_2O_3 FETs with T_{ch} of (a) 1.2 nm, (b) 1.6 nm, and (c) 2.0 nm. The $R_{sh,n}$ and $R_{sh,+}$ near $V_{GS}{\sim}V_T$ (V_T from the devices with L_{ch} = 1 μm) are highlighted in orange arrows to emphasize their differences. (d) Extracted R_C as a function of V_{GS} for In_2O_3 transistors with T_{ch} ranging from 1.2 to 2.0 nm. R_C are extracted based on the short L_{ch} TLM analysis. (e) Schematic band diagrams of metal/In_2O_3 contacts for different In_2O_3 thicknesses. E_C: conduction band minimum, CNL: CNL of In_2O_3, and E_{FM}: metal Fermi level.

1.2 nm), a positive Φ_{SB} forms at the metal/In_2O_3 contact. Conversely, when E_C falls below CNL (as seen for $T_{ch} \geq$ 1.6 nm), Φ_{SB} becomes negative. This transition in Φ_{SB} with increasing T_{ch} from 1.2 nm to above 1.6 nm has been studied and corroborated in our earlier work [25].

Fig. 6(a) presents the extracted ΔL as a function of V_{GS}, calculated using (4). The ΔL values at $V_{GS}{\sim}V_T$, ranging from 0.30 to 0.73 μm, are highlighted for reference. Fig. 6(b) shows the relationship between V_T and L_{ch} for different T_{ch}. As previously discussed in Fig. 2, all devices exhibit significant V_T roll-off, even when L_{ch} remains larger than 5 × λ. Notably, the L_{ch} at which V_T roll-off begins aligns well with the extracted ΔL values at $V_{GS}{\sim}V_T$ [Fig. 6(a) and (b)], substantiating the impact of the CDE on V_T roll-off. The relatively large ΔL values further explain why V_T roll-off occurs even when L_{ch} is much greater than the natural length (5 × λ = 10–15 nm) of the transistors. When $L_{ch} > \Delta L$, reducing L_{ch} has minimal impact on V_T, as the carrier density at the channel center stays unaffected by the n^+ regions extending from the S/D contacts [like Fig. 3(c)]. However, when $L_{ch} \leq \Delta L$, the n^+ regions from the S/D begin to merge, increasing the carrier density at the channel center [like Fig. 3(b)]. This results in a negative shift of V_T and a pronounced V_T roll-off as L_{ch} decreases.

B. Mechanisms Behind the CDE

The high carrier density n^+ regions beneath the S/D electrodes, referred to as the CDE, have been identified as a key factor contributing to the V_T roll-off of In_2O_3 FETs in the previous section. The remaining questions are: what causes this CDE in In_2O_3 transistors, and why do S/D metals increase the carrier density in the underlying In_2O_3? In this work,

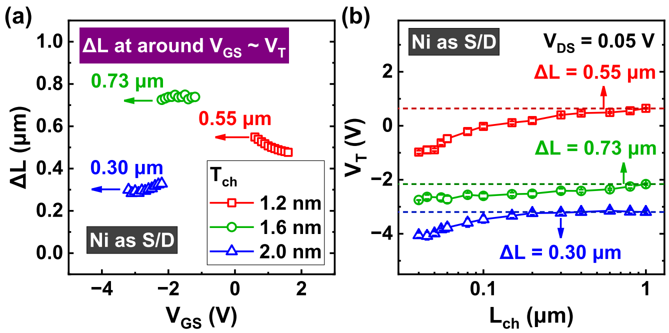

Fig. 6. (a) Extracted ΔL as a function of V_{GS} for In_2O_3 FETs with T_{ch} ranging from 1.2 to 2.0 nm. The ΔL values at $V_{GS}{\sim}V_T$ are highlighted for reference. (b) Linearly extrapolated V_T as a function of L_{ch}. Each data point represents the average of at least five devices. All T_{ch} In_2O_3 FETs exhibit a clear V_T roll-off phenomenon, even when L_{ch} is still significantly larger than $5 \times \lambda$, suggesting that the CDE might influence the V_T behavior. The ΔL values at $V_{GS}{\sim}V_T$ are marked in the figure and show good consistency with the L_{ch} at which the V_T roll-off begins.

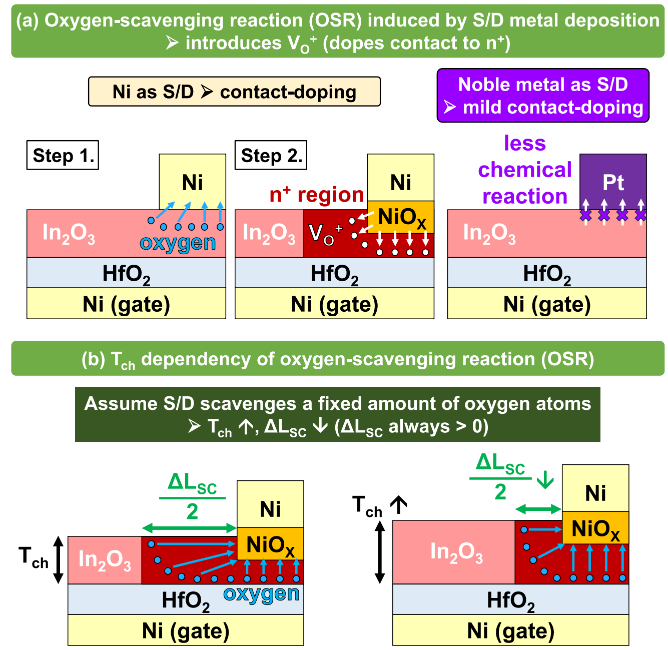

Fig. 7. (a) Schematic illustration of the oxygen-scavenging reaction (OSR) induced by the S/D metal. When a metal such as Ni is deposited on In_2O_3, it may react with In_2O_3 and scavenge oxygen atoms from the channel. Oxygen vacancies (V_O^+) are generated during the OSR process. In contrast, using noble metals like Pt as S/D can suppress the OSR. (b) Schematic representation of the T_{ch}-dependent OSR effect, where $\Delta L_{SC}/2$ denotes the length of the n^+ region formed due to the OSR from the source or drain metal. The total length of n^+ region from S/D is ΔL_{SC}.

we propose two mechanisms that may contribute to the contact doping in In_2O_3 FETs. The first one is oxygen-scavenging reactions (OSR) at the metal/In_2O_3 S/D contacts (Fig. 7), and the second one is the change in the sign of the Φ_{SB} at metal/In_2O_3 interface (Fig. 8). These mechanisms provide insight into why CDE, quantified by ΔL, depends on the T_{ch} of In_2O_3, as shown in Fig. 6(a). When Ni is deposited as the S/D metal, it may react with In_2O_3, scavenging oxygen atoms from the channel. This scavenging process generates oxygen vacancies (V_O^+) in the In_2O_3 channel [Fig. 7(a)]. Since V_O^+ acts as a shallow donor and directly correlates with the carrier density in doped In_2O_3 (such as IGZO and ITO) and pure In_2O_3 [4], [6], [9], [32], the introduction of V_O^+ via OSR increases electron density, forming n^+ regions near the S/D contacts. The length of the n^+ region induced by OSR is denoted as ΔL_{SC}, as illustrated in Fig. 7(b). For the same type of S/D metal, assuming a consistent amount of oxygen is scavenged from the In_2O_3 channel, the product $\Delta L_{SC} \times T_{ch}$—which is proportional to the total number of oxygen atoms involved in the scavenging reactions—should remain similar. Consequently, in thinner T_{ch} devices, ΔL_{SC} must be longer than in thicker T_{ch} transistors to provide sufficient oxygen atoms for the scavenging reaction.

The Φ_{SB} at the metal/In_2O_3 interface also influences the carrier density beneath the S/D contacts, as illustrated in Fig. 8. When $\Phi_{SB} > 0$, electrons near the contact are depleted due to the upward band bending at $V_{GS} = V_T$, forming a depletion region with width $= W_{dep}$ [Fig. 8(a)]. This depletion effect counteracts the OSR-induced carrier increase, potentially leading to n^- rather than n^+ regions in In_2O_3. Conversely, when $\Phi_{SB} < 0$, the metal/In_2O_3 interface accumulates electrons due to downward band bending [22], creating an accumulation region with width $= W_{acc}$ [Fig. 8(b)]. Defining ΔL_{SBH} as the length of the n^+ region induced by the Φ_{SB} from S/D, a positive Φ_{SB} at $T_{ch} = 1.2$ nm results in $\Delta L_{SBH} < 0$, reducing the n^+ region length generated from OSR. Meanwhile, a negative Φ_{SB} at $T_{ch} \geq 1.6$ nm leads to $\Delta L_{SBH} > 0$, expanding the n^+ region. The overall dependencies of ΔL, ΔL_{SC}, and ΔL_{SBH} on T_{ch} are summarized in Fig. 9, where ΔL is determined by the sum of ΔL_{SC} and ΔL_{SBH} ($\Delta L = \Delta L_{SC} + \Delta L_{SBH}$). Fig. 9 explains the ΔL–T_{ch} relationship observed in Fig. 6. Note that the impact of Φ_{SB} on ΔL is constrained by the small values of W_{dep} and W_{acc}, leading to a relatively minor $|\Delta L_{SBH}|$. As a result, the Φ_{SB} effect on ΔL and V_T may be overshadowed unless OSR at the S/D contact is mitigated—an aspect that will be further explored in Figs. 10 and 11.

Since OSR plays a critical role in the CDE, there are two effective strategies to reduce the OSR and improve the V_T roll-off caused by the CDE in In_2O_3 FETs. These strategies also reinforce the idea that OSR is a key contributor to CDE and V_T roll-off. The first approach is using O_2 annealing or O_2 plasma treatments to reduce the V_O^+ generated by the OSR, a method that has been well-studied in our previous works [4], [24]. The second approach involves replacing the S/D metals with noble metals, such as Pt, which should experience less OSR with In_2O_3 [as illustrated in Fig. 7(a)]. Therefore, noble metals are expected to alleviate the V_T roll-off issue and reduce the CDE. Fig. 10 presents the transfer characteristics of In_2O_3 FETs with different L_{ch}, $T_{ch} = 1.2$, 1.6, and 2.0 nm, and Pt as the S/D metal. Fig. 11 shows the V_T–L_{ch} dependencies extracted from the I_D–V_{GS} curves in Fig. 10. When compared to devices with Ni as S/D [Fig. 2 for transfer curves and Fig. 6(b) for V_T–L_{ch} dependency], In_2O_3 FETs with Pt as the S/D metal clearly exhibits improved V_T roll-off as the L_{ch} decreases. This supports the hypothesis that OSR at the S/D interfaces contributes significantly to the V_T roll-off and CDE in In_2O_3 transistors.

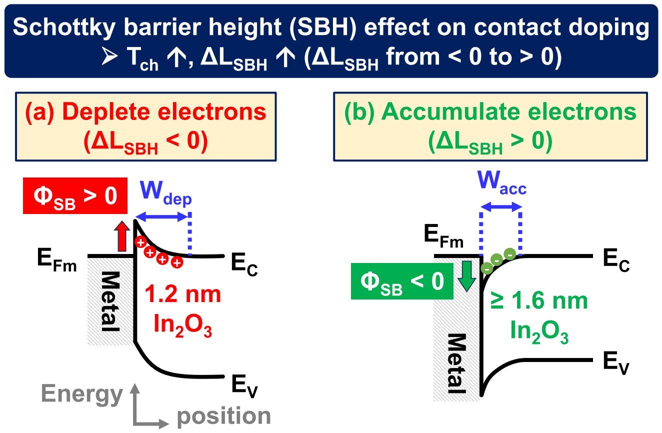

Fig. 8. Schematic band diagrams of metal/In_2O_3 contacts for (a) T_{ch} = 1.2 nm (with $\Phi_{SB} > 0$) and (b) $T_{ch} \geq 1.6$ nm (with $\Phi_{SB} < 0$) at $V_{GS} = V_T$. The length of the n^+ regions induced by the Φ_{SB} at the metal/In_2O_3 contacts is denoted as ΔL_{SBH}. A positive Φ_{SB} depletes electrons at the interface, creating a depletion region with a width W_{dep}, which counteracts the carrier increase caused by OSR at the S/D contacts ($\Delta L_{SBH} < 0$). In contrast, a negative Φ_{SB} leads to electron accumulation, contributing to an accumulation width W_{acc}, which further intensifies the CDE in the In_2O_3 channel ($\Delta L_{SBH} > 0$). Since In_2O_3 is an n-type semiconductor, W_{acc} is inherently smaller than W_{dep}.

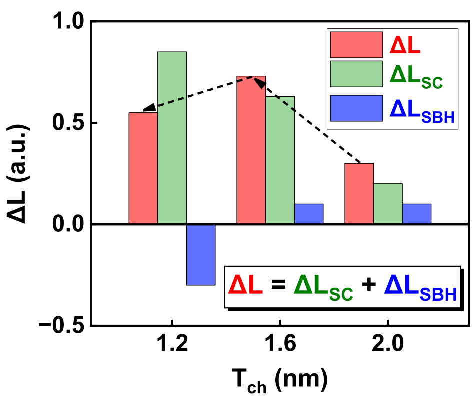

Fig. 9. Summary of the T_{ch} dependencies of ΔL, ΔL_{SC}, and ΔL_{SBH}, where $\Delta L = \Delta L_{SC} + \Delta L_{SBH}$. The values of ΔL_{SC} and ΔL_{SBH} are estimated for qualitative understanding of their T_{ch} dependencies and may involve some degree of inaccuracy.

Interestingly, In_2O_3 devices with Pt as S/D and T_{ch} = 1.2 nm exhibit an unusual V_T roll-up as the L_{ch} scales down (Fig. 11), which contrasts sharply with the typical V_T roll-off seen in the devices with Ni as S/D and T_{ch} = 1.2 nm [Fig. 6(b)]. Normally, OSR dominates the influence of Φ_{SB} on the CDE in In_2O_3 transistors. However, with Pt as the S/D metal, where OSR is largely suppressed, Φ_{SB} becomes the dominant factor affecting the V_T–L_{ch} relationship. For T_{ch} = 1.2 nm devices, where $\Phi_{SB} > 0$, the upward band bending profile forms a depletion region and depletes electrons from the Pt/In_2O_3 contact [Fig. 8(a)]. As the L_{ch} decreases, the depletion regions near the S/D start to influence the electron density at the In_2O_3 channel center, resulting in the observed V_T roll-up in Fig. 11. For $T_{ch} \geq 1.6$ nm devices, the negative Φ_{SB} with downward band bending has less effect on the V_T–L_{ch} dependency (Fig. 11) because the accumulation region width [W_{acc}, as shown in Fig. 8(b)] is not long enough to affect the channel center when $L_{ch} \geq 40$ nm.

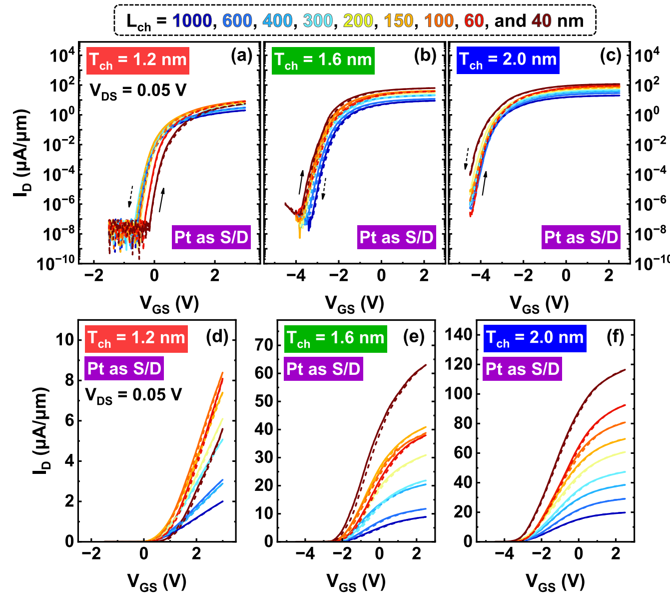

Fig. 10. Transfer characteristics of In_2O_3 transistors with Pt as the S/D metal, featuring L_{ch} ranging from 1 μm to 40 nm and T_{ch} of 1.2 nm [(a): I_D in log scale; (d): I_D in linear scale], 1.6 nm [(b): I_D in log scale; (e): I_D in linear scale], and 2.0 nm [(c): I_D in log scale; (f): I_D in linear scale]. Solid lines represent forward V_{GS} sweeps, while dashed lines indicate backward sweeps. Compared to In_2O_3 FETs with Ni as the S/D metal (Fig. 2), devices using Pt exhibit a milder V_T roll-off.

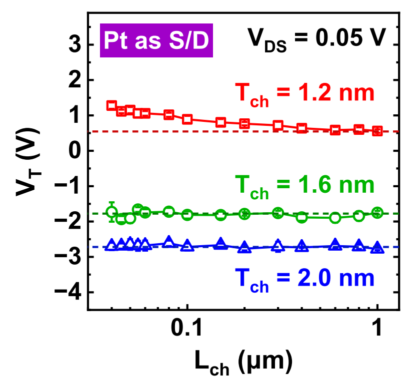

Fig. 11. Linearly extrapolated V_T as a function of L_{ch} of In_2O_3 FETs with Pt as S/D and various T_{ch}. Each data point represents the average of at least five devices.

In addition to Pt and Ni, other metals, such as Al, Ti, and Pd, are also used as the S/D electrodes in In_2O_3 transistors to investigate their impact on the V_T roll-off. Fig. 12(a) summarizes the V_T–L_{ch} dependencies for In_2O_3 FETs with these different S/D metals. Except for the devices using Pt as the S/D, all the other transistors exhibit significant V_T roll-off as the L_{ch} decreases. To understand these observations, the oxygen interstitial formation energies for various metals are simulated by *ab initio* calculations using QuantumATK, as shown in Fig. 12(b). The oxygen interstitial formation energy indicates how easily a material reacts with oxygen atoms: a lower formation energy suggests that the material is more likely to react with oxygen. Therefore, at the metal/In_2O_3 interface, if the metal has a smaller oxygen interstitial formation energy than In, the oxygen atoms in In-O bonds will preferentially react with the metal, rather than staying in the

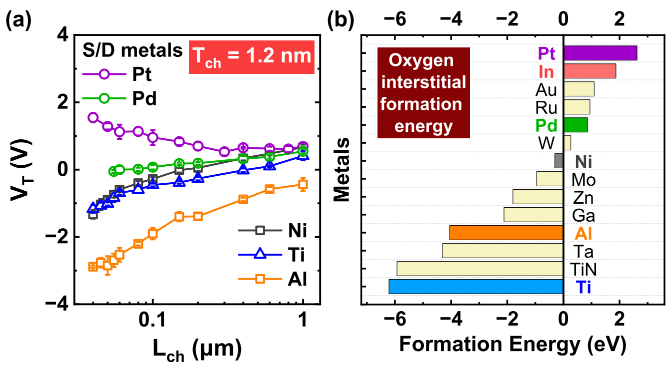

Fig. 12. (a) Linearly extrapolated V_T as a function of L_{ch} for In_2O_3 FETs with various metals as S/D and T_{ch} = 1.2 nm. Each data point represents the average of at least five devices. A broad range of metals were examined to assess their impact on the V_T roll-off in In_2O_3 transistors. (b) Simulated formation energies of oxygen interstitials in various metals. The energies were simulated by *ab initio* calculations using QuantumATK. Metals with smaller formation energies are more likely to react with oxygen.

In_2O_3, which leads to OSR. In Fig. 12(b), Pt is the only metal with a larger oxygen interstitial formation energy than In, meaning it does not scavenge oxygen from In_2O_3, and thus does not contribute to CDE and V_T roll-off. In contrast, metals like Pd, Ni, Al, and Ti have lower formation energies versus In, which facilitates the OSR at the metal/In_2O_3 interface. The fact that many metals tend to have OSR with In-O bonds also explains why the V_T roll-off phenomenon is commonly observed not only in In_2O_3 FETs [4], [22], [23], [24], [25] but also in other doped In_2O_3 transistors like InSnO (ITO) [6], [26], IZO [18], IGO [12], and IGZO devices [9], [27], [31]. Notably, all these studies have used S/D metals (such as Ni, TiN, and Mo) with low oxygen interstitial formation energies.

IV. Conclusion

In summary, this work systematically investigates the CDE and its impact on the V_T roll-off issue in In_2O_3 FETs. The CDE describes the increase in carrier density near the S/D electrodes, forming n^+ regions, which leads to a non-uniform carrier concentration profile along the In_2O_3 channel. By analyzing long L_{ch} and short L_{ch} devices separately, we extract $R_{sh,n}$, $R_{sh,+}$, and ΔL to quantify the CDE. The strong correlation between ΔL and the L_{ch} where V_T roll-off begins suggests that the V_T roll-off in In_2O_3 transistors is caused not by the traditional SCE but by the CDE. Next, the underlying mechanisms of the CDE are explored. It is found that the OSR that occurs when depositing the S/D metals on the In_2O_3 channel is one of the reasons contributing to the CDE. The S/D metals may scavenge oxygen atoms from In_2O_3, generating oxygen vacancies and increasing the carrier density near the S/D. This OSR mechanism is verified through experiments with different S/D metals and simulations of oxygen interstitial formation energy. Additionally, the Schottky barrier height (Φ_{SB}) at the metal/In_2O_3 contacts also has minor influences on the CDE. Positive Φ_{SB} (when T_{ch} = 1.2 nm) depletes carriers, while negative Φ_{SB} (when $T_{ch} \geq 1.6$ nm) accumulates carriers at the In_2O_3 channel beneath the S/D electrodes. This research offers new insights into the CDE and its crucial role in the V_T roll-off behavior of OS transistors. It lays the foundation for future studies aimed at mitigating CDE and improving the performance of In_2O_3 and other In_2O_3-based transistors.

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